IN THE CLAIMS

Please amend the claims as follows.

1. (Currently Amended) A computer-implemented method of initializing a simulation comprising:

accessing an attribute on a simulation model within a simulation of a self-resetting circuit; and

responsive to the attribute, conditionally treating an unknown state of an input node on the simulation model as a known state.

2. (Original) The computer-implemented method of claim 1 wherein conditionally treating an unknown state comprises:

when the attribute is set, evaluating an output node of the simulation model using the known state for the input node rather than the unknown state.

3. (Original) The computer-implemented method of claim 2 wherein evaluating an output node comprises detecting an X on the input node, and evaluating the output node as if a 0 was on the input node.

4. (Original) The computer-implemented method of claim 3 wherein the simulation model is a model of an inverter, and evaluating an output node comprises detecting an X on the input node, and evaluating the output node to a 1.

5. (Original) The computer-implemented method of claim 2 wherein evaluating an output node comprises detecting an X on the input node, and evaluating the output node as if a 1 was on the input node.

6. (Original) The computer-implemented method of claim 5 wherein the simulation model is a switch-level model of a transistor, and evaluating an output node comprises detecting an X on a gate node of the switch-level model of the transistor, and logically closing the switch-level model of the transistor.

Claims 7-15. (Canceled)

16. (Currently Amended) An article having a computer readable medium, the computer readable medium having instructions stored thereon for performing a method of initializing a device model in a simulation, the method comprising:

accessing an attribute of the device model within a simulation of a self-resetting circuit to ascertain a state of the attribute; and

responsive to the state of the attribute, conditionally treating an X on an input node of the device model as a value other than an X.

17. (Original) The article of claim 16 wherein the attribute is associated with the input node, the method further comprising:

accessing a second attribute of the device model, the second attribute being associated with a second input node; and

responsive to a state of the second attribute, conditionally treating an X on the second input node as a value other than an X.

18. (Original) The article of claim 16 wherein conditionally treating comprises:

conditionally treating an X on any input node of the device model as a value other than an X.

19. (Original) The article of claim 16 wherein the device model is a model of an inverter, the simulation is a switch-level simulation, and conditionally treating comprises:

when the attribute is set and an X is present on an input node to the model of the inverter, evaluating an output node of the model of the inverter to a 1.

20. (Original) The article of claim 16 wherein the device model is a model of an inverter, the simulation is a switch-level simulation, and conditionally treating comprises:

when the attribute is set and an X is present on an input node to the model of the inverter, evaluating an output node of the model of the inverter to a 0.

Claims 21-25. (Canceled)

26. (New) The computer-implemented method of claim 1 wherein the self-resetting circuit comprises:

a first P-channel transistor having a source coupled to a voltage supply and a drain;

a second P-channel transistor having a source coupled to the voltage supply and a drain;

a first inverter having an input coupled to the drain of the first P-channel transistor and the drain of the second P-channel transistor and an output coupled to a gate of the second P-channel transistor;

a second inverter having an input coupled to the gate of the second P-channel transistor and an output coupled to a gate of the first P-channel transistor; and

an N-channel transistor having a drain coupled to the drain of the first P-channel transistor and the drain of the second P-channel transistor and a source coupled to ground.

27. (New) The article of claim 16 wherein the device model is a model of a transistor, the simulation is a switch-level simulation, and conditionally treating comprises:

when an X is present on a gate node of the model of the transistor, logically closing the model of the transistor.

28. (New) The article of claim 16 wherein the self-resetting circuit comprises:

a first P-channel transistor having a source coupled to a voltage supply and a drain;

a second P-channel transistor having a source coupled to the voltage supply and a drain;

a first inverter having an input coupled to the drain of the first P-channel transistor and the drain of the second P-channel transistor and an output coupled to a gate of the second P-channel transistor;

a second inverter having an input coupled to the gate of the second P-channel transistor and an output coupled to a gate of the first P-channel transistor; and

an N-channel transistor having a drain coupled to the drain of the first P-channel transistor and the drain of the second P-channel transistor and a source coupled to ground.

29. (New) A computer-implemented method of initializing a simulation comprising:

accessing a first attribute on a simulation model within a simulation of a self-resetting circuit;

responsive to the first attribute, conditionally treating an unknown state of a first input node on the simulation model as a known state;

accessing a second attribute on the simulation model within the simulation; and

responsive to the second attribute, conditionally treating an unknown state of a second input node on the simulation model as a known state.

30. (New) The computer-implemented method of claim 29, further comprising evaluating an output node of the simulation model as a function of a state of the first input node and a state of the second input node.

31. (New) The computer-implemented method of claim 29 wherein the simulation model is a model of a logic function.

32. (New) The computer-implemented method of claim 29 wherein the simulation model is a model of an AND gate, an OR gate, a NAND gate, or a NOR gate.

33. (New) The computer-implemented method of claim 29, further comprising:

when the first attribute is set, interpreting an unknown state of the first input node as a logical zero; and

when the second attribute is set, interpreting an unknown state of the second input node as a logical zero.

34. (New) The computer-implemented method of claim 29, further comprising:

when the first attribute is set, interpreting an unknown state of the first input node as a logical one; and

when the second attribute is set, interpreting an unknown state of the second input node as a logical one.